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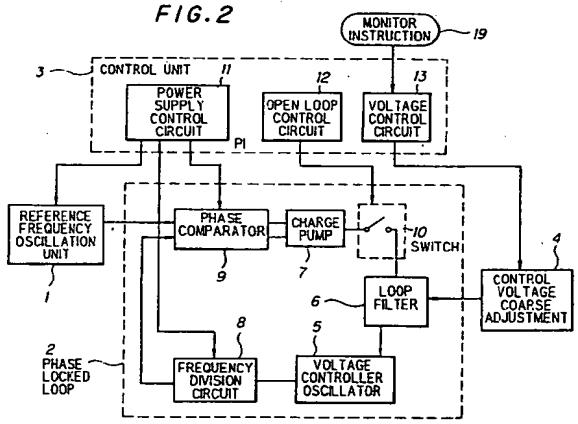
(54) Frequency synthesizer.

(57) A control voltage coarse adjustment circuit (4) including a D/A converter voltage generator (15) is provided on a load side of a capacitor in a loop filter (6) included in a phase locked loop (2). A coarsely adjusted voltage is thus generated and added to a voltage generated by the capacitor of the loop filter for the switch-over of channels during a communication frame.

The added voltages are applied to a voltage controlled oscillator (5) to change its frequency for the switch-over of channels. Consequently, the charge and discharge of the capacitor is carried out in a short time and suppresses the influence of dielectric absorption current. Thus, the intermittent operation of the phase locked loop (6) in which the phase locked loop is closed and opened intermittently is carried out for the saving of electric power consumption, and a carrier frequency is stabilized in the open phase locked loop by an electric charge voltage of the capacitor in the loop filter.

FIG.2



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The invention relates to a frequency synthesizer, and more particularly to, a power saving type of a local oscillation frequency synthesizer to be used in a TDMA (time division multiplexing access) system.

In a TDMA system, an adjacent cell is monitored during an idle slot in a communication frame by changing a frequency from a presently using channel to a channel which is considered to be appropriate in the adjacent cell, and the formerly used channel is restored by changing again the frequency. For this purpose, a technology in which the switch-over of oscillation frequencies is carried out with high speed is required in the TDMA system.

A conventional frequency synthesizer used in a TDMA system comprises a reference frequency oscillation unit for generating a reference frequency dependent on a carrier frequency, a voltage controlled oscillator for generating a carrier frequency dependent on an applied control voltage, a frequency division circuit for dividing the carrier frequency by a fixed division ratio, a phase comparator for comparing the reference frequency and a divided carrier frequency to provide a phase difference therebetween, a charge pump for charging and discharging a capacitor by receiving the phase difference, and a loop filter having a capacitor to be charged pump for generating the control voltage to be applied to the voltage controlled oscillator, wherein the voltage controlled oscillator, the frequency division circuit, the phase comparator, the charge pump and the loop filter are connected to provide a phase locked loop which is closed and opened by a loop on/off switch.

In operation, the loop on/off switch is turned on, and a power supply voltage is applied to the reference frequency oscillation unit, and the frequency division circuit and the phase comparator in the phase locked loop, so that the voltage controlled oscillator is applied with a control voltage from the loop filter having the capacitor which is charged and discharged dependent on the phase difference detected in the phase comparator by the charge pump. Thus, a controlled carrier frequency is generated in the voltage controlled oscillator. Then, the loop on/off switch is turned off to make the phase locked loop open, and the power supply voltage is not applied to the reference frequency oscillation unit, and the frequency division circuit and the phase comparator in the opened phase locked loop, so that the voltage controlled oscillator is maintained to generate a carrier frequency which is determined by an electric charge voltage of the capacitor in the loop filter. Thus, the phase locked loop is controlled to operate intermittently, thereby realizing the saving of electric power.

In the conventional frequency synthesizer used in a TDMA system, the reference frequency is changed dependent on a controlled carrier frequency obtained in the voltage controlled oscillator, so that the switch-over of channels having a small step width is carried out, while a frequency division ratio of the frequency division circuit is suppressed to be low. Consequently, the switch-over of frequencies is realized with high speed.

However, the conventional frequency synthesizer has a disadvantage in that the loop intermittent operation for the electric power saving is limited to be carried out during a period in which the switch-over of channels is not performed, because the turning-off of the loop on/off switch to provide the loop intermittent operation is difficult to be carried out subsequently to the voltage stabilization of the capacitor in the loop filter under the situation where the switch-over of channels is performed in a TDMA system by a short period. In more detail, the capacitor in the loop filter is frequently charged and discharged at a communication frame, during which synchronism is set up with a separated frequency for the switch-over of channels, by the charge pump. In this situation, the capacitor takes a time in realizing the voltage stabilization due to the occurrence of dielectric absorption current flowing in the capacitor immediately after the charge and discharge thereof.

Accordingly, it is an object of the invention to provide a frequency synthesizer in which the intermittent operation of a phase locked loop is carried out with a sufficient time at a communication frame.

It is a further object of the invention to provide a frequency synthesizer in which the intermittent operation fo a phase locked loop to be carried out at a communication frame is realized without inviting a complicated circuit structure.

According to the invention, a frequency synthesizer, comprises:

a reference signal oscillation unit for providing a reference signal;

a phase locked loop comprising a voltage controlled oscillator for generating a carrier frequency dependent on a control voltage applied thereto, a frequency division circuit for dividing the carrier frequency to provide a divided frequency by a predetermined division ratio, a phase comparator for comparing the reference frequency and the divided frequency to provide a phase difference, a charge pump for applying a charging voltage and a discharging voltage to a nodal point, a loop filter having a capacitor connected to the nodal point for generating the control voltage to be applied to the voltage controlled oscillator, and a loop on/off switch for closing and opening the phase locked loop;

a control unit comprising a power supply con-

trol circuit for applying an operative voltage to the phase locked loop which is closed by the loop on/off switch which is turned on intermittently for a switch-over of channels, a closed loop control circuit for controlling the loop on/off switch to be turned on and off in accordance with intermittent operation of the phase locked loop, and a voltage control circuit for controlling and application of a coarsely controlled voltage to the voltage controlled oscillator for the switch-over of channels in a communication frame; and

a control voltage coarse adjustment circuit for generating the coarsely controlled voltage to be added to the control voltage of the capacitor in the loop filter by a control of the voltage control circuit.

The invention will be explained in more detail in conjunction with appended drawings, wherein:

Fig. 1 is a block diagram showing a conventional frequency synthesizer to be used in a TDMA system,

Fig. 2 is a block diagram showing a frequency synthesizer in a preferred embodiment according to the invention,

Fig. 3 is a block diagram showing a voltage control circuit for a loop filter in the preferred embodiment,

Fig. 4 is an explanatory diagram showing a relation between a communication frame in a TDMA system and an oscillation frequency required in the preferred embodiment.

Before explaining a frequency synthesizer in a preferred embodiment according to the invention, the aforementioned conventional frequency synthesizer to be used in a TDMA system will be explained in Fig. 1.

The conventional frequency synthesizer comprises a reference frequency unit 1 for generating a reference frequency, a phase locked loop 2 for equalizing a carrier frequency to the reference frequency, and a control unit 3 for controlling the reference frequency unit 1 and the phase locked loop 2 to operate.

The reference frequency unit 1 comprises a direct digital synthesizer 17 and a clock oscillator 18, wherein a reference frequency which is dependent on a predetermined carrier frequency is digitally obtained in accordance with a fixed clock frequency supplied from the clock oscillator 18 by the direct digital synthesizer 17.

The phase locked loop 2 comprises a voltage controlled oscillator 5 for generating a carrier frequency dependent on applied control voltage, a loop filter 6 having a capacitor for generating a control voltage to be applied to the voltage controlled oscillator 5, a charge pump 7 for charging the capacitor in the loop filter 6 by receiving a phase difference between the reference frequency and a divided frequency of the carried frequency, a frequency division circuit 8 for providing the divided frequency of the carried frequency, a phase comparator 9 for providing the charge pump 7 with the phase difference, and a loop on/off switch 10 for closing and opening the phase locked loop 2.

The control unit 3 comprises a voltage control circuit 11 for applying a power supply voltage to the reference frequency unit 1, and the frequency division circuit 8 and the phase comparator 9 in the phase locked loop 2 when the phase locked loop 2 is closed for the phase locking operation, and an open loop control circuit 12 for closing and opening the phase locked loop 2 intermittently in synchronism with the intermittent application of the power supply voltage by the voltage control circuit 11.

Operation and a disadvantage of the conventional frequency synthesizer have been formerly explained.

Therefore, the explanation thereof is not made here.

Next, a frequency synthesizer in the preferred embodiment according to the invention will be explained in Figs. 2 to 4, wherein like parts are indicated by like reference numerals as used in Fig. 1.

In Figs. 2 and 3, there is added to the conventional frequency synthesizer a control voltage coarse adjustment circuit 4 comprising a D/A converter-voltage generator 15 for generating a coarse-adjustment voltage and a capacitor 16 connected in parallel between a capacitor 14 of the loop filter 6 and ground, wherein the loop filter 6 comprises the capacitor 14 and resisters R1 and R2, and the control unit 3 comprises a voltage control circuit 13 for controlling the control voltage coarse adjustment circuit 4 by receiving a monitor instruction 19 additionally to the conventional structure.

Fig. 4 shows a communication frame of 20ms in a TDMA system comprising a receiving slot 21, a transmitting slot 22 and an idle slot 23. In the idle slot 23, a carrier frequency 20 is changed from a frequency f_1 for a channel presently used for a communication including the receiving slot 21 and the transmitting slot 22 to a frequency f_2 for a channel to be considered appropriate in an adjacent cell. Then, when the carrier frequency f_2 is not appropriate for a communication as a result of monitoring the adjacent cell, the carrier frequency f_2 is restored for the subsequent communication. Only in such cases as changing the carrier frequencies f_1 and f_2, a phase lock loop is closed, and a power supply voltage is applied thereto. On the other hand, when it is not necessary to change a carrier frequency, that is, a carrier frequency set up by an electric charge voltage of the capacitor 14 in the loop filter 6 and a voltage of the D/A converter voltage generator 15 is maintained, no power supply voltage is applied to the phase locked loop

2 which is opened by the loop on/off switch 10.

Thus, the intermittent operation is realized to save electric power consumption.

In operation, a carrier frequency of the voltage controlled oscillator 5 is maintained by a voltage obtained in the addition fo an electric charge voltage of the capacitor 14 in the loop filter 6 and a voltage of the D/A converter voltage generator 15 in accordance with the control of the voltage control circuit 13, under the situation where the synchronism is set up with a predetermined carrier frequency of a communication channel.

Here, when the voltage control circuit 13 receives a monitor instruction 19, by which the carrier frequency is changed to a carrier frequency of an adjacent cell at the idle slot 23 in the communication frame to check a receiving sensitivity of the adjacent cell, the voltage control circuit 13 controls the control voltage coarse adjustment circuit 4 to change a voltage of the D/A converter voltage generator 15 by a changing amount of ΔV which is defined below.

$$\Delta V = \alpha \times (f_1 - f_2)$$

Where f_1 is a frequency of a presently using communication channel, f_2 is a frequency of a channel to be monitored, and α is a modulation sensitivity.

Thus, a voltage applied to the voltage controlled oscillator 5 by the loop filter 6 is coarsely adjusted by the control voltage coarse adjustment circuit 13, and a finely controlled voltage is applied from the loop filter 6 to the voltage controlled oscillator 5 by a phase difference of the phase comparator 9. Consequently, the intermittent operation of the phase locked loop becomes possible to be carried out for the electric power saving, because the capacitor 14 of the loop filter 16 becomes stabilized in a short time even during a remaining short period at the communication frame after the setting-up of synchronism with a carrier frequency.

The changing amount of the capacitor 16 in the control voltage coarse adjustment circuit 13 is small in an electric charge voltage between before and after the switch-over of channels, so that the influence of dielectric absorption current becomes negligible in the preferred embodiment. Therefore, a control voltage applied to the voltage controlled oscillator 5 becomes stabilized in a time sufficiently shorter than that in the conventional frequency synthesizer, so that an electric charge voltage is maintained without transient change, even if the loop on/off switch 10 is turned off to make the phase locked loop open. Consequently, a carrier frequency obtained by the voltage controlled oscillator 5 is maintained to be a predetermined value in cooperation with a voltage of the D/A converter voltage generator 15 in the intermittent operation of the phase locked loop 2.

After the adjacent cell is monitored, the frequency is changed back to a carrier frequency for the communication channel in the state where the loop on/off switch 10 is turned on to make the phase locked loop 2 close. For this purpose, an output voltage of the D/A converter voltage generator 15 is coarsely changed to comply with a communical channel by the control voltage-coarse adjustment circuit 13, and a voltage of the capacitor 14 is finely changed to provide the setting-up of synchronism with a carrier frequency of the communication channel by the charge pump 7 receiving a phase difference from the phase comparator 9.

Although the invention has been described with respect to specific embodiment for complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modification and alternative constructions that may be occur to one skilled in the art which fairly fall within the basic teaching herein set forth.

Claims

1. A frequency synthesizer, comprising:

a reference signal oscillation unit for providing a reference signal;

a phase locked loop comprising a voltage controlled oscillator for generating a carrier frequency dependent on a control voltage applied thereto, a frequency division circuit for dividing said carrier frequency to provide a divided frequency by a predetermined division ratio, a phase comparator for comparing said reference frequency and said divided frequency to provide a phase difference, a charge pump for applying a charging voltage and a discharging voltage to a nodal point, a loop filter having a capacitor connected to said nodal point for generating said control voltage to be applied to said voltage controlled oscillator, and a loop on/off switch for closing and opening said phase locked loop;

a control unit comprising a power supply control circuit for applying an operative voltage to said phase locked loop which is closed by said loop on/off switch which is turned on intermittently for a switch-over of channels, a closed loop control circuit for controlling said loop on/off switch to be turned on and off in accordance with intermittent operation of said phase locked loop, and a voltage control circuit for controlling an application of a coarsely controlled voltage to said voltage controlled oscillator for said switch-over of channels in a

communication frame; and

a control voltage coarse adjustment circuit for generating said coarsely controlled voltage to be added to said control voltage of said capacitor in said loop filter by a control of said voltage control circuit.

2. A frequency synthesizer, according to claim 1, wherein;

said loop on/off switch is positioned at said nodal point.

3. A frequency synthesizer, according to claim 1 or 2, wherein;

said control voltage coarse adjustment circuit comprises a D/A converter voltage generator and a capacitor in parallel connected between a negative terminal of said capacitor in said loop filter and ground, said D/A converter voltage generator controlled to receive a digital value to generate said coarsely controlled voltage by said voltage control circuit.

FIG.1 PRIOR ART

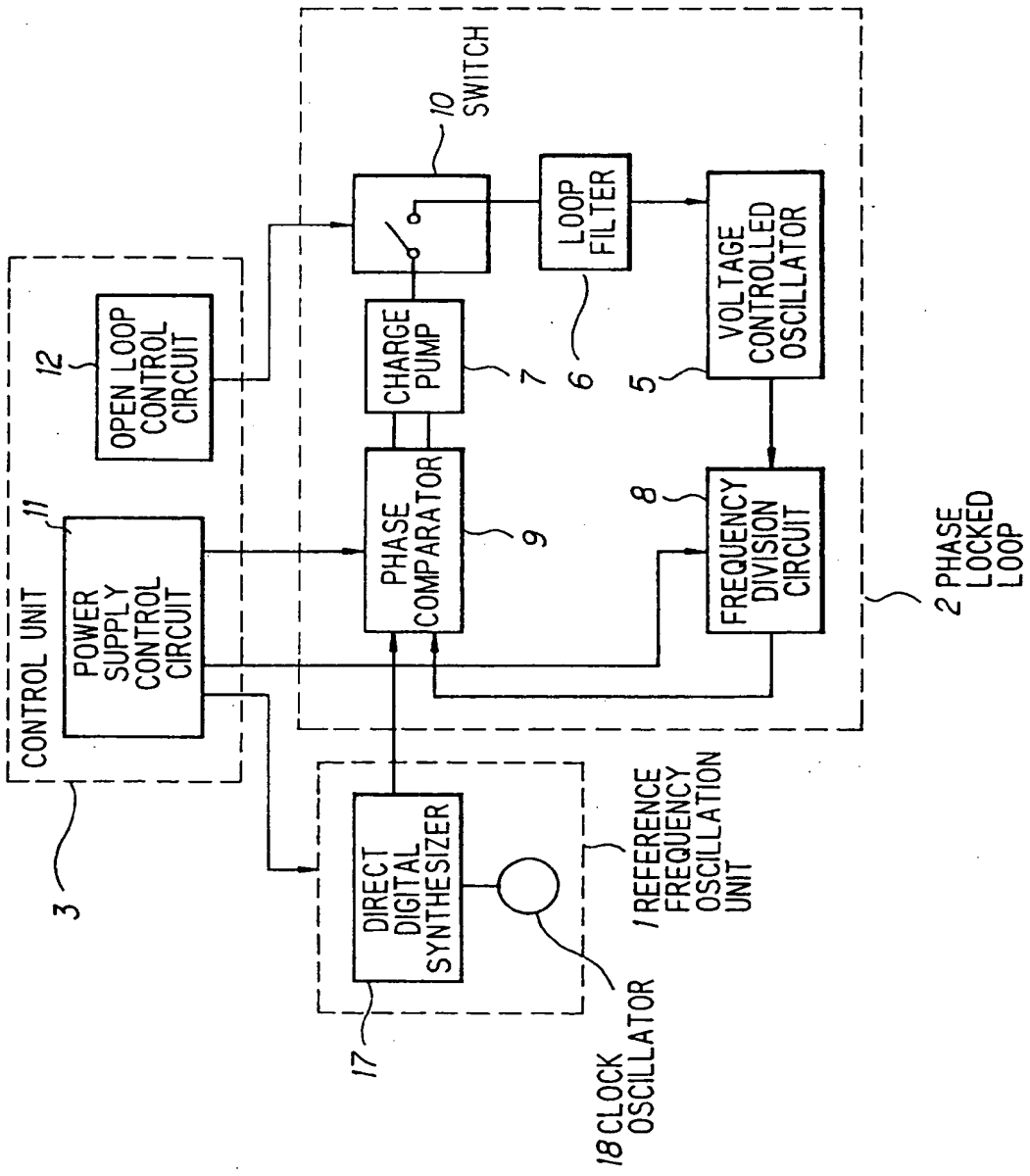


FIG. 2

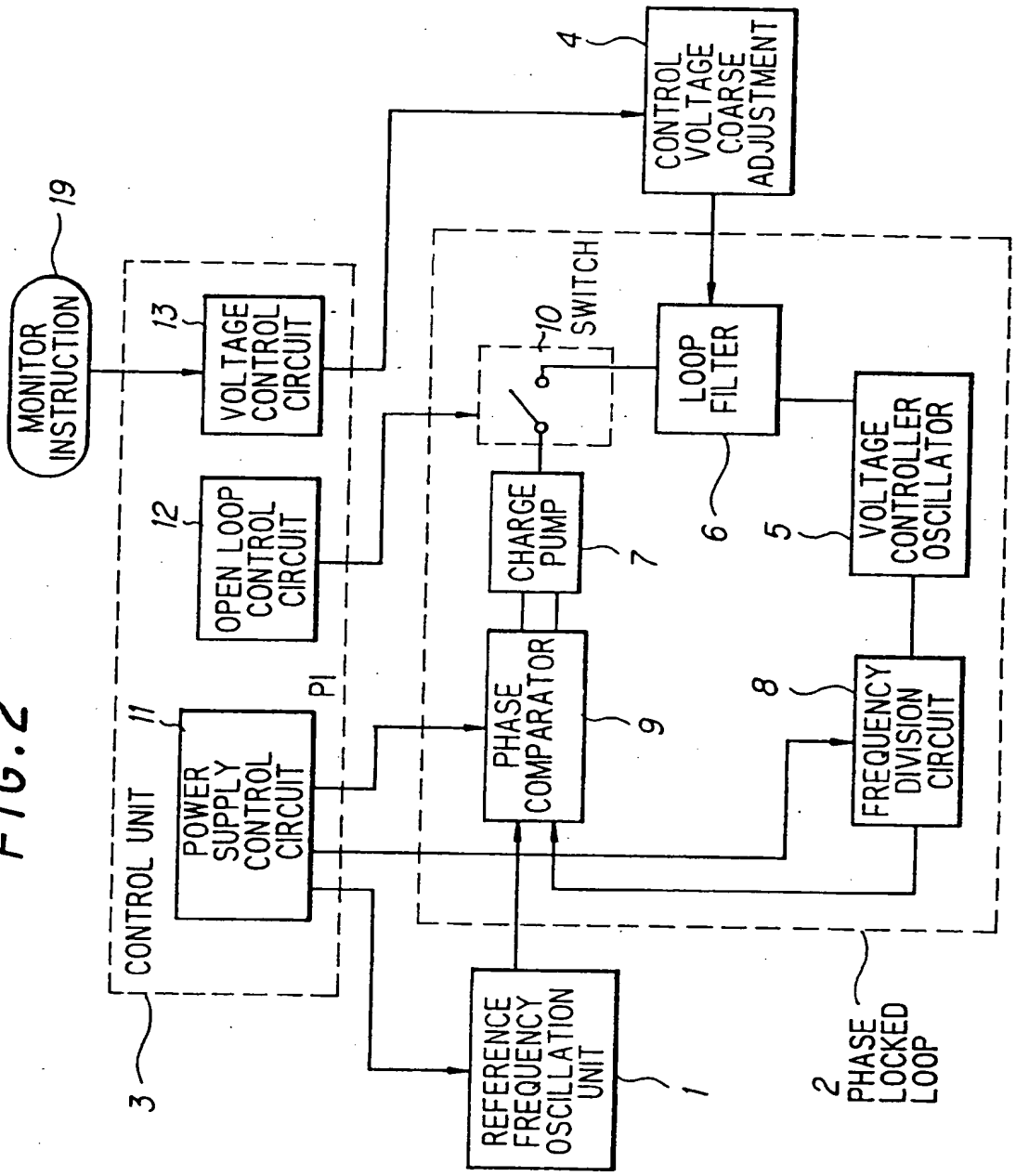

MONITOR INSTRUCTION
19
VOLTAGE CONTROL CIRCUIT
13
CONTROL VOLTAGE COARSE ADJUSTMENT
4
SWITCH
10
LOOP FILTER
6
OPEN LOOP CONTROL CIRCUIT
12
CHARGE PUMP
7
VOLTAGE CONTROLLER OSCILLATOR
5
CONTROL UNIT
11
POWER SUPPLY CONTROL CIRCUIT
PI
PHASE COMPARATOR
9
8
FREQUENCY DIVISION CIRCUIT
REFERENCE FREQUENCY OSCILLATION UNIT
1
3
2
PHASE LOCKED LOOP

FIG. 3

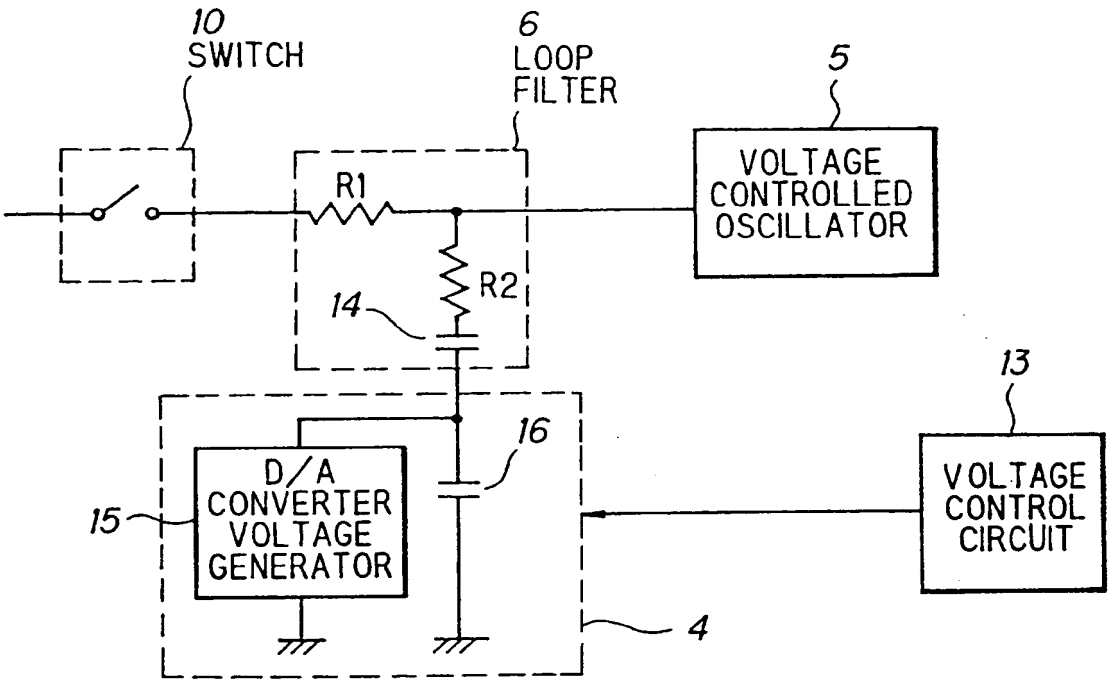
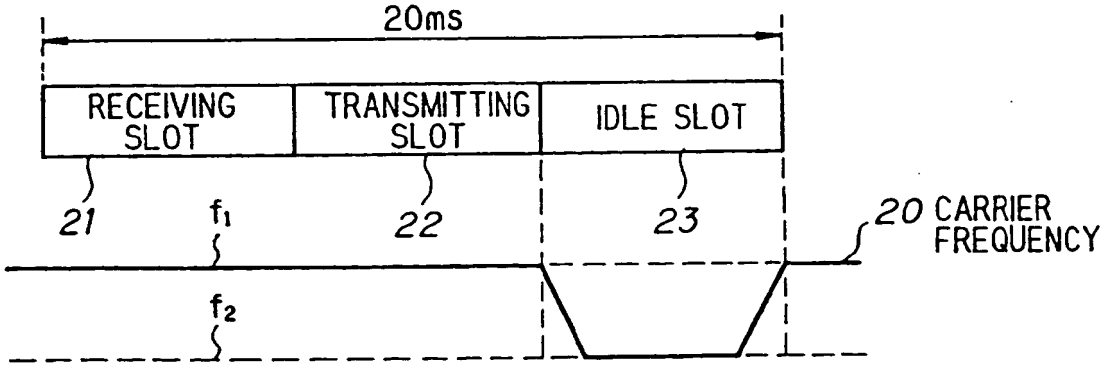

10
SWITCH
6
LOOP
FILTER
5
VOLTAGE
CONTROLLED
OSCILLATOR
R1
R2
14
13
16
D/A
CONVERTER
VOLTAGE
GENERATOR
15
VOLTAGE
CONTROL
CIRCUIT
4

FIG. 4


20ms
RECEIVING
SLOT
TRANSMITTING
SLOT
IDLE SLOT
21
22
23
f1
f2
20 CARRIER
FREQUENCY

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 11 0261

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	CH-A-677 298 (FIRMA ERIKA KÖCHLER) * column 4, line 7 - column 5, line 32; figure 3 *	1-3	H03L7/14 H03L7/189
Y	EP-A-0 360 442 (NIPPON TELEGRAPH AND TELEPHONE CORPORATION) * page 7, line 4 - line 14; figure 8 * * page 7, line 25 - line 56; figures 10-12 * * page 8, line 4 - line 24; figure 14 * * page 8, line 57 - line 58; figure 18 * * page 9, line 5 - line 9; figure 20 *	1-3	
A	NTT REVIEW vol. 4, no. 1, January 1992, TOKYO JP pages 64 - 69 , XP292915 ISAO SHIMIZU ET AL. 'NEW DIGITAL MOBILE RADIO TECHNOLOGIES' * page 67, paragraph 2.4; figure 7 *	1-3	
A	EP-A-0 471 502 (FUJITSU LIMITED) * column 1, line 17 - line 26 * * column 5, line 32 - column 11, line 44; figures 4-9 *	1-3	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	07 OCTOBER 1993	BALBINOT H.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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